**Cell Description:**This is a standard single-bit, negative-edge triggered flip-flop with an asynchronous, active low clear signal. The input signal to this cell is sampled on the falling edge of the clock signal, and both the sampled signal and its compliment are provided at the output of the cell.

**Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **CLK** | **D** | **CLRBAR** | **Q** |  |
| 0 | 0 | 0 | 0 |  |
| 0 | 0 | 1 | 0 |  |
| 0 | 1 | 0 | 1 |  |
| 0 | 1 | 1 | Q |  |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | Q |  |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | Q |  |

**Behavioral Verilog:**

//Verilog HDL for "Lib6710\_06", "DFFNEGCLK" "behavioral"

module DFFNEGCLK( Q, QB, CLRB, CLK, D );

input CLRB;

input CLK;

input D;

output reg Q;

output QB;

assign QB = ~Q;

always@(negedge CLK or negedge CLRB)

begin

if(~CLRB)

Q <= 1'b0;

else

Q <= D;

end

specify

(D => Q) = (1.0, 1.0);

(D => QB) = (1.0, 1.0);

(CLK => Q) = (1.0, 1.0);

(CLK => QB) = (1.0, 1.0);

(CLRB => Q) = (1.0, 1.0);

(CLRB => QB) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| DFFNEGCLKX1 | 27.0 | 48 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFNEGCLKX1 |  |  |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFNEGCLKX1 |  |  |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFNEGCLKX1 |  |  |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| DFFNEGCLKX1 |  |  |

**Logic Symbol:**

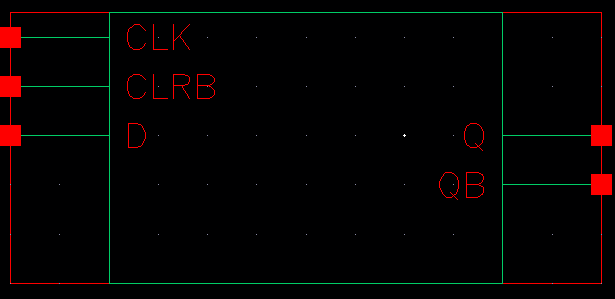
****

Figure : Symbol View for the DFFNEGCLK cell.

**CMOS Schematic:**

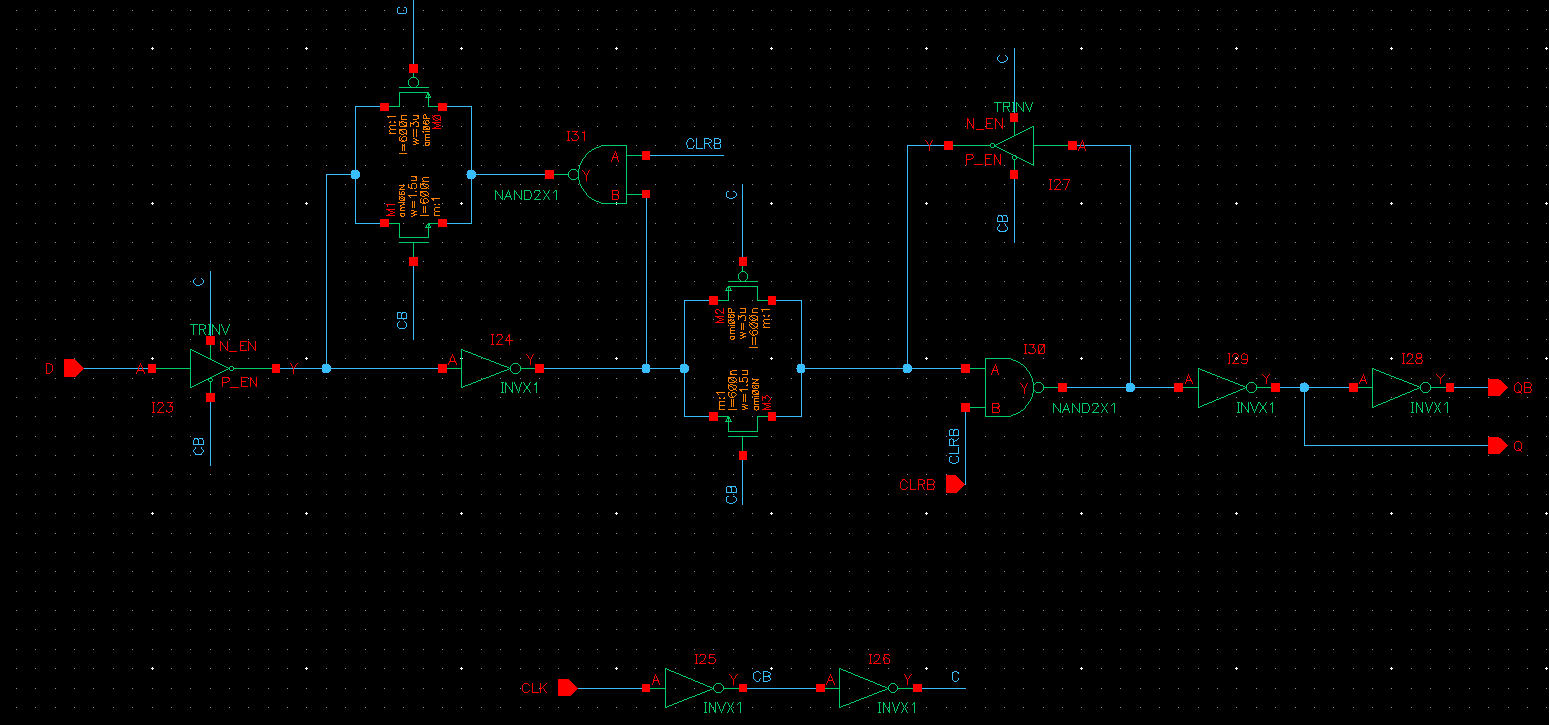
****

Figure : CMOS schematic for the DFFNEGCLKX1 Cell

**CMOS Layout:**

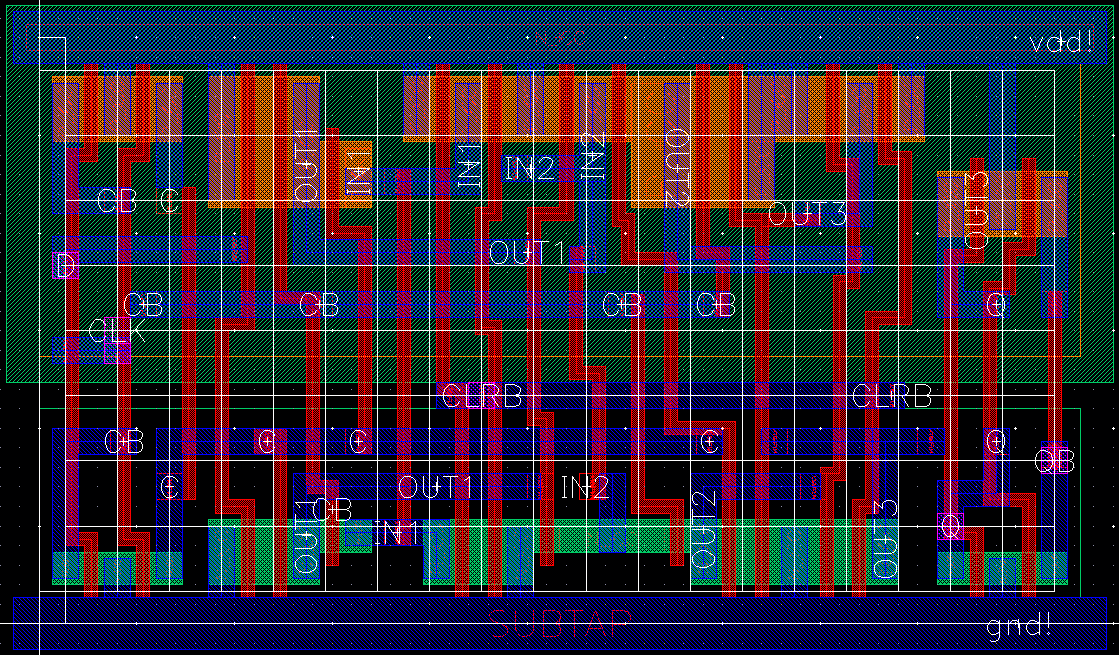
****

Figure : CMOS layout for the DFFNEGCLKX1 cell.